## IN THE SPECIFICATION

**Please replace paragraph [0001] with the following:**

**[0001]** This application is a divisional of United States Patent Application Serial No. 10/073,723 filed February 11, 2002 ~~and~~, titled, "FET HAVING EPITAXIAL SILICON GROWTH," ~~(allowed),~~ and issued as U.S. Patent No. 6,716,687 on April 6, 2004, which application is commonly assigned and incorporated herein by reference. The present invention is related to United States Patent Application Serial No. 09/713,844 to Abbott et al., titled "METHOD OF FORMING A FIELD EFFECT TRANSISTOR," filed November 15, 2000, issued as US 6,599,789 on July 29, 2003, which is commonly assigned and incorporated herein by reference.

**Please replace paragraph [0020] with the following:**

**[0020]** Referring to Figure 1C, a dielectric, or insulative, material 20 is deposited over masking material 16 and within and overfilling trenches 18 and 19. Exemplary and preferred processing includes sidewall oxidation ~~either~~ before ~~or after~~ deposition of layer 20. ~~For a further embodiment, the sidewall oxidation may be performed prior to formation of layer 16.~~ For one embodiment, the material for layer 20 is high-density plasma deposited oxide. The dielectric material is preferably initially deposited to overfill the trenches and then subsequently planarized at least to masking material 16 to provide the construction as illustrated in Figure 1C. Example planarizing techniques include chemical-mechanical polishing (CMP) and resist etch-back.

**Please replace paragraph [0030] with the following:**

**[0030]** Referring to Figure 1I, a gate 34 is formed over channel region 14. Preferably as shown, a gate dielectric layer 36, for example silicon dioxide, is first formed over channel region 14. A gate stack is then formed over channel region 14. For one embodiment, the gate stack includes a conductively doped polysilicon layer 38 and a conductive silicide layer 40 (for example $WSi_x$) and a nitride capping layer 42. Thereafter, at least one pocket implanting is conducted to provide at least one pocket implant region intermediate source/drain semiconductive material 26, forming region 30/32, and channel region 14. In the illustrated and preferred example, exemplary pocket implants include source/drain extension (SDE) implant regions 44 having a thickness of approximately 500 Angstroms, and halo implant regions 46 provided therebeneath having an approximate thickness of 500 Angstroms and to extend below

source/drain regions 30 and 32. Insulative spacers are subsequently added as shown. Rapid thermal processing is preferably conducted at some point, as is conventional.